CLAIMS

1. An apparatus for testing one or more processors, the apparatus comprising:

a host computer means for suspending the one or more processors and controlling the input to the one or more processors, the host computer comprising an interface means; and

a test motherboard means connected to the host computer means via the interface means, and configured for receiving and interfacing to the one or more processors; wherein the interface means transfers signals of the host computer means to and from the test motherboard means.

2. The apparatus of Claim 1, wherein the test motherboard means further comprises a bus interface means for translating signals used by the host computer to signals used by the one or more processors, and for translating signals used by the one or more processors to signals used by the host computer means.

3. The apparatus of Claim 1, wherein the test motherboard means further comprises:

an Arbiter and Traffic Generator means for controlling a motherboard bus on the test motherboard means;

an I/O Chipset means for providing at least one PCI connection to connect to the interface means;

a bus interface means for translating between the motherboard bus signals and bus signals used by the one or more processors; and

one or more socket means for receiving the one or more processors.

4. An apparatus for testing one or more processors, the apparatus comprising:

a host computer means using a first bus architecture for suspending the one or more processors and controlling the input to the one or more processors using a second bus architecture, the host computer comprising an interface means; and

a test motherboard means coupled to the host computer means via the interface means, the test motherboard means further comprising:

one or more socket means for receiving the one or more processors;

an arbiter means using the first bus architecture for controlling the bus of the test motherboard means;

an I/O means for providing a connection between the interface means and the test motherboard means; and

a bus interface means for interfacing to the one or more processors, and for translating between the first bus architecture and the second bus architecture.

5. The apparatus of Claim 4, wherein the first bus architecture is PCI.

6. The apparatus of Claim 4, wherein the test motherboard means further comprises:

a memory means for storing at least one of data and instructions; and

a test interface means for interfacing with at least one of a logic analyzer and a debugger.

7. The apparatus of Claim 4, wherein the test motherboard means further comprises:

a memory means for storing at least one of data and instructions; and

a test interface means for interfacing with at least one of a logic analyzer and a debugger; wherein at least one of the bus interface means, the one or more sockets, the memory means, and the test interface means is placed on a test daughterboard means.

8. A method of providing test case information to one or more processors, the method comprising the steps of:

suspending by a host computer the one or more processors;

issuing by the host computer the test case information to be performed by the one or more processors, the host computer operating in a first architecture;

transferring by an interface the test case information to a test motherboard;

translating the test case information from the first architecture to a second architecture, the second architecture being used by the one or more processors; and

performing by the one or more processors the test case information.

9. The method of Claim 8, further comprising the steps of:

replacing the second architecture with a third architecture, the third architecture being used by a second one or more processors;

translating the test case information from the first architecture to the third architecture; and

performing by the second one or more processors the test case information.

10. An apparatus for providing test case information to one or more processors, the apparatus comprising:

means for suspending by a host computer the one or more processors;means for issuing by a host computer the test case information to be performed by the one or more processors, the host computer operating in a first architecture;

means for transferring by an interface the test case information to a test motherboard;

means for translating the test case information from the first architecture to a second architecture, the second architecture being used by the one or more processors; and

means for performing by the one or more processors the test case information.

11. The apparatus of Claim 10, further comprising:

means for replacing the second architecture with a third architecture, the third architecture being used by a second one or more processors;

means for translating the test case information from the first architecture to the third architecture; and

means for performing by the second one or more processors the test case information.

12. A computer program product for providing test case information to one or more processors, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer program code for suspending by a host computer the one or more processors;

computer program code for issuing by the host computer the test case information to be performed by the one or more processors, the host computer operating in a first architecture;

computer program code for transferring by an interface the test case information to a test motherboard;

computer program code for translating the test case information from the first architecture to a second architecture, the second architecture being used by the one or more processors; and

computer program code for performing by the one or more processors the test case information.

13. The computer program product of Claim 12, further comprising the steps of:

computer program code for replacing the second architecture with a third architecture, the third architecture being used by a second one or more processors;

computer program code for translating the test case information from the first architecture to the third architecture; and

computer program code for performing by the second one or more processors the test case information.